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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,539	09/29/2003	Frank A. Baiocchi	1-1-36-5	1844

7590 01/25/2005

Ryan, Mason & Lewis, LLP
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Locust Valley, NY 11560

EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,539	BAIOCCHI ET AL.	
	Examiner	Art Unit	
	Renee R Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) 10-18 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-9 and 19-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 and 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,521,923 to D'Anna in view of US Patent No. 6,372,557 to Leong.

In regards to claims 1 and 19, D'Anna teaches a metal-oxide-semiconductor (MOS) device, comprising: a semiconductor layer of a first conductivity type; a first source/drain region of a second conductivity-type formed in the semiconductor layer; a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region; a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions at column 12, lines 19-36; and at least one contact, the at least one contact comprising: a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and at least one insulating layer formed directly on the silicide layer at column 9, lines 17-31.

In regards to claim 8, D'Anna teaches the device of claim 1, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a

source region and the second source/drain region comprises a drain region at column 6, lines 14-16 and 34-37.

In regards to claim 9, D'Anna teaches the device of claim 8, wherein the MOS device comprises a lateral DMOS (LDMOS) device at column 6, lines 14-16.

In regards to claim 20, D'Anna teaches the IC device of claim 19, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions at column 9, lines 58-65.

In regards to claim 24, D'Anna teaches the IC device of claim 19, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region at column 6, lines 50-55.

However, D'Anna does not teach all the limitations of the claims.

In regards to claims 1 and 2, Leong teaches the device of claim 1, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n- type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions at column 5, lines 54-59, claim 1.

In regards to claim 3, Leong teaches the device of claim 1, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer at column 6, lines 38-56, claim 10.

In regards to claim 4, Leong teaches the device of claim 1, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer at column 4, lines 16-20.

In regards to claim 5, Leong teaches the device of claim 1, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device at column 4, lines 7-15.

In regards to claim 6, Leong teaches the device of claim 1, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate at column 6, lines 5-21.

In regards to claims 7 and 23, Leong teaches the device of claim 1, wherein the first source/drain region comprises a source region and the second source/drain region comprises a drain region at column 6, lines 2-4, claim 4.

In regards to claim 21, Leong teaches the IC device of claim 19, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer at column 6, lines 11-21, claim 5.

In regards to claim 22, Leong teaches the IC device of claim 19, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer at column 4, lines 16-20.

In regards to claim 25, Leong teaches the IC device of claim 19, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device at column 4, lines 7-10.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified D'Anna to include the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n- type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions; substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the

semiconductor layer; at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer; and a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate, since such a modification would result in minimized resistance, as described in column 1, lines 56-63 of Leong.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RRB

January 24, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 and 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. in view of US Patent No..

In regards to claim 1, teaches a metal-oxide-semiconductor (MOS) device, comprising: a semiconductor layer of a first conductivity type; a first source/drain region of a second conductivity-type formed in the semiconductor layer; a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region; a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and at least one contact, the at least one contact comprising: a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and at least one insulating layer formed directly on Ihe silicide layer.

In regards to claim 2, teaches the device of claim 1, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n- type and p-type regions such that the silicide layer

forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

In regards to claim 3, teaches the device of claim 1, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer.

In regards to claim 4, teaches the device of claim 1, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

In regards to claim 5, teaches the device of claim 1, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device.

In regards to claim 6, teaches the device of claim 1, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

In regards to claim 7, teaches the device of claim 1, wherein the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

In regards to claim 8, teaches the device of claim 1, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

In regards to claim 9, teaches the device of claim 8, wherein the MOS device comprises a lateral DMOS (LDMOS) device.

In regards to claim 19, teaches an integrated circuit (1C) device comprising a plurality of metal-oxide semiconductor (MOS) devices, at least one of the MOS devices comprising: a semiconductor layer of a first conductivity type; a first source/drain region of a second conductivity type formed in the semiconductor layer; a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region; a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and at least one contact, the at least one contact comprising: a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and at least one insulating layer formed directly on the silicide layer.

In regards to claim 20, teaches the IC device of claim 19, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

In regards to claim 21, teaches the IC device of claim 19, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer.

In regards to claim 22, teaches the IC device of claim 19, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

In regards to claim 23, teaches the IC device of claim 19, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

In regards to claim 24, teaches the IC device of claim 19, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

In regards to claim 25, teaches the IC device of claim 19, wherein the silicide layer fonns a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device.